

Level shifter circuit

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Abstract

A level shifter circuit of the preferred embodiment can be used as a transfer gate driver of a memory circuit such as a DRAM. A pair of cross-coupled transistors receives a first potential. A plurality of transistors are coupled between the pair of cross-coupled transistors and a second potential. An output unit has a pull-down switch for providing an output signal of one of first, second and third potentials and are coupled to the pair of cross-coupled transistor and the plurality of transistors. The third potential has a potential between the first and second potentials

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Kim(10) Patent No.: **US 6,222,384 B1**
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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) Int. Cl.⁷ **H03K 19/0175; H03K 19/094**(52) U.S. Cl. **326/68; 326/81; 365/189.11**(58) Field of Search 326/81, 80, 82,
326/83, 68, 59, 60; 365/189.11(56) **References Cited****U.S. PATENT DOCUMENTS**

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Primary Examiner—Michael Tokar*Assistant Examiner*—Daniel D. Chang(74) *Attorney, Agent, or Firm*—Fleshner & Kim, LLP(57) **ABSTRACT**

A level shifter circuit of the preferred embodiment can be used as a transfer gate driver of a memory circuit such as a DRAM. A pair of cross-coupled transistors receives a first potential. A plurality of transistors are coupled between the pair of cross-coupled transistors and a second potential. An output unit has a pull-down switch for providing an output signal of one of first, second and third potentials and are coupled to the pair of cross-coupled transistor and the plurality of transistors. The third potential has a potential between the first and second potentials.

13 Claims, 5 Drawing Sheets